Notice of Allowability	Application No.	Applicant(s)	
	10/724,534	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/31/2007*.

2. ☒ The allowed claim(s) is/are *1-6,8-20,31,33,37-40,42-44,50 and 51*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/31/2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALFORD KINDRED
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

CONTINUED EXAMINATION UNDER 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/2007 has been entered.

I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

2. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated October 31, 2007 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be

filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

4. Authorization for this examiner's amendment was given in a telephone interview with James Ausley, having Reg. No. 49,076, on December 12, 2007. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

5. The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

In claim 1, lines 4-5, "the instructions can be performed out of an original program order as part of a predicted branch" is replaced with -the instructions are performed out of an original program order for at least one predicted branch-.

In claim 1, line 11, "capable of performing" is replaced with -for performing-.

In claim 12, lines 4-5, "the instructions can be performed out of an original program order as part of a predicted branch" is replaced with -the instructions are performed out of an original program order for at least one predicted branch-.

In claim 31, line 7, "the processing circuit can process the arithmetic and logic instructions" is replaced with -the processing circuit processes at least some of the arithmetic and logic instructions-.

III. DISTINGUISHING FEATURES RECITED IN THE CLAIMS

ALLOWABLE SUBJECT MATTER

6. Claims 1-6, 8-20, 31, 33, 37-40, 42-44 and 50-51 are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, **See MPEP 1302.14**:

The primary reasons for allowance of claim 1 in the instant application is the combination with the inclusion in the claim that there are "**... routing a series of assembly instructions to a processor having a first execution circuit for executing arithmetic and logic instructions, wherein the instructions are performed out of an original program order for at least one predicted branch that has not yet been taken; analyzing the series of assembly instructions to detect a search instruction to perform a search operation, the search instruction comprising a data string and a starting address for the search operation; routing the search instruction undecoded to a data**

string manipulation circuit, independent of the first execution circuit, for performing string manipulation instructions; routing the starting address for the search operation from the data string manipulation circuit to a cache memory array; comparing portions of the data string with consecutive portions of data stored in the cache memory array; generating a match signal for each portion of the data stored in the cache memory array that matches a respective compared portion of the data string; identifying a plurality of match signals indicating the consecutive portions of the data stored in the cache memory array that together match the data string; monitoring data dependencies among the instructions; and routing an address of cached data matching the data string to the data string manipulation circuit, wherein the routing the address of cached data matching the data string is performed after any instructions are performed that modify data within the address ..." The prior art of record including the disclosures of Hsu et al. (US Patent 5,948,100) and Simcoe (US Patent 6,000,008) neither anticipates nor renders obvious the above recited combination. Because claims 2-6, 8-11 and 50 depend directly or indirectly on claim 1, these claims are considered allowable for at least the same reasons noted above.

The primary reasons for allowance of claim 12 in the instant application is the combination with the inclusion in the claim that there are "**... routing a series of instructions to a processor having a general execution circuit for**

executing arithmetic and logic instructions, wherein the instructions are performed out of an original program order for at least one predicted branch that has not yet been taken; analyzing the series of instructions to detect a search instruction to perform a search operation, the search instruction comprising a starting address and a data string; routing the search instruction to a data string manipulation circuit without intervention by the general execution circuit; routing the starting address for the search operation from the data string manipulation circuit to a cache memory; searching a cache line in the cache memory for data that matches the data string, wherein said cache line comprises more bytes than the data string; monitoring data dependencies regarding blocks of addresses among the instructions; and routing an address of cached data matching the data string to the data string manipulation circuit, wherein the routing the address of cached data matching the data string is performed after any instructions are performed that modify data within the address ..." The prior art of record including the disclosures of Hsu et al. (US Patent 5,948,100) and Simcoe (US Patent 6,000,008) neither anticipates nor renders obvious the above recited combination. Because claims 13-20 depend directly or indirectly on claim 12, these claims are considered allowable for at least the same reasons noted above.

The primary reasons for allowance of claim 31 in the instant application is the combination with the inclusion in the claim that there are "**... a data memory**

comprising a plurality of cache lines, each cache line comprising a plurality of bytes of data; an instruction fetch circuit; a first instruction processing circuit coupled to the instruction fetch circuit and configured to perform arithmetic and logic instructions received from the instruction fetch circuit and wherein the processing circuit processes at least some of the arithmetic and logic instructions out of an original program order as part of a predicted branch that has not yet been taken; a second instruction processing circuit coupled to the instruction fetch circuit and configured to monitor data dependencies regarding blocks of addresses among the instructions and to perform data string operations such that data string instructions are issued after completion of arithmetic and logic instructions that modify data in associated source or destination address blocks of the data memory, the second instruction processing circuit being further configured to receive a data string and an instruction to perform a search operation beginning at a starting source or destination address of the data memory, the second instruction processing circuit further comprising: a plurality of inputs coupled to the data memory such that each input is coupled to receive a different one of the plurality of bytes of data of the Cache line, and a plurality of comparators, each comparator coupled to a respective one of the plurality of inputs and configured to compare the byte of data of the cache line received by the respective input with a portion of the data string, each comparator further configured to generate a match signal when the byte of data matches the compared portion of the data

string, the plurality of comparators further comprising a plurality of outputs; and a decoder circuit coupled to the plurality of outputs to receive match signals from the plurality of comparators and configured to identify sequential portions of the cache line having data that, when combined, matches the data string ..." The prior art of record including the disclosures of Hsu et al. (US Patent 5,948,100) and Simcoe (US Patent 6,000,008) neither anticipates nor renders obvious the above recited combination. Because claims 33 and 37-39 depend directly on claim 31, these claims are considered allowable for at least the same reasons noted above.

The primary reasons for allowance of claim 40 in the instant application is the combination with the inclusion in the claim that there are "**... a cache data memory means for holding at least one cache line comprising a plurality of bytes of data; means for searching the at least one cache line for a data value, wherein said means for searching is coupled to said cache data memory means, and wherein said means for searching receives a starting address for a search operation of the at least one cache line and aligns the data value with an offset of the starting address to search multiple portions of the at least one cache line in one clock cycle for data that matches compared portions of the data value; means for detecting a string of matches between the multiple portions of the at least one cache line and the compared portions of the data value; means for performing arithmetic and logic operations including out of an original program order as part of a**

predicted branch that has not yet been taken; means for monitoring data dependencies of blocks of addresses corresponding to the operations; and means for receiving a series of instructions, wherein said means for receiving is coupled to both said means for searching and said means for performing, said means for receiving being further configured to forward a first instruction associated with the search operation to said means for searching and to forward second instructions associated with arithmetic and logic operations to said means for performing, wherein second instructions that modify data associated with the data value are performed before first instructions associated with the data value ..." The prior art of record including the disclosures of Hsu et al. (US Patent 5,948,100) and Simcoe (US Patent 6,000,008) neither anticipates nor renders obvious the above recited combination. Because claims 42-44 and 51 depend directly or indirectly on claim 40, these claims are considered allowable for at least the same reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

IV. CLOSING COMMENTS

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 17, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

ALFORD KINDRED
SUPERVISORY PATENT EXAMINER